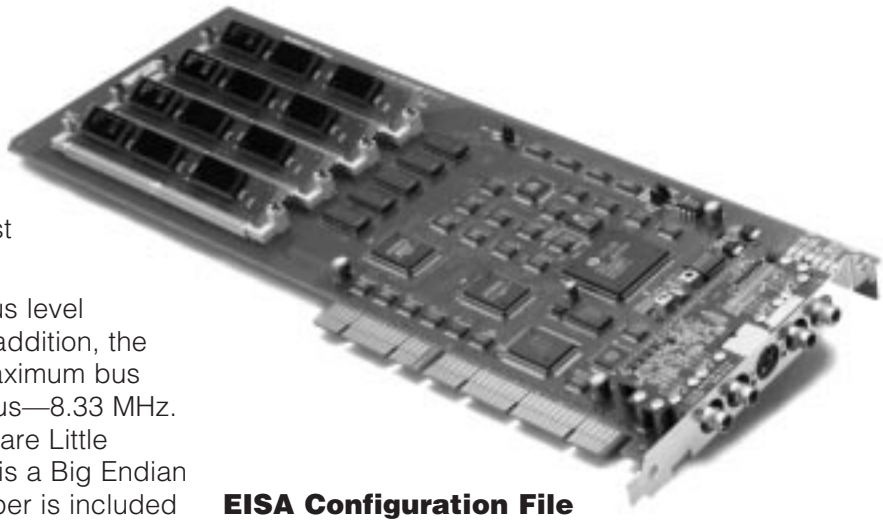
EISA



The SCRAMNet+ EISA interface board is compatible with any PC or workstation with an available 32-bit EISA board slot. Its compact ASIC design fits into a single slot in the host computer's chassis.

The SCRAMNet+ EISA supports bus level interrupts IRQ 10, 11, 12, and 15. In addition, the SCRAMNet+ EISA operates at the maximum bus clock speed allowable by the EISA bus—8.33 MHz. Since most EISA bus based systems are Little Endian processors and SCRAMNet+ is a Big Endian network, a hardware-level byte swapper is included in the SCRAMNet+ EISA card that enhances the system compatibility.

Memory

Address: The replicated shared memory can be located anywhere in the extended memory portion of EISA space.

Data: Data transfers to the SCRAMNet+ EISA memory can be 8, 16 or 32 bits wide. The host interface card is a 32-bit card.

Control and Status Registers

EISA SPECIAL REGISTER: The SCRAMNet+ EISA card has 11 special registers that control features of the SCRAMNet+ card that are particular to the EISA bus or that are required to be in a separate address space to comply with the EISA specification. The registers are set via the EISA configuration utility. The CSRs base address is slot specific. The CSRs require 64 Bytes of contiguous space. Data transfers to the CSRs on the SCRAMNet+ EISA bus host interface can be either 8, 16, or 32 bits wide.

EISA Configuration File

The SCRAMNet+ EISA card has its own configuration file registered with BSPR Services, Inc. under the product identifier SCR. This file contains the information used by the EISA configuration utility necessary to set-up the SCRAMNet+ EISA card.

Interrupt Capability

The following interrupt levels are supported: 10,11,12,15. Edge triggered input is set via the supplied SCRAMNet+ EISA configuration file for each of the supported interrupt levels. One IRQ level is required for memory interrupts and one IRQ level is required for status interrupts. They must be different.

Byte Swapping

The EISA SCRAMNet+ card is equipped with a hardware based byte swapping facility so that it can easily communicate with Big Endian computers. This facility is engaged by setting a bit in the EISA special registers. The swapping occurs based on the length of the read/write transaction.

SPECIFICATIONS

Hardware Compatibility
- EISA 32-bit compliant; version 3.11
- EISA max. bus clock speed is 8.33 MHz

Physical Dimensions
13.000˝ x 5.000˝ (330.200 mm x 127.000 mm)

Weight
.600 lb. (272.160 g.)

Electrical Requirements
+5 VDC, 1.5 Amps

Shared-Memory Sizes
4 KB or 128 KB (on-board) which can be upgraded to 512 KB, 1 MB, 2 MB, 4 MB, or 8 MB using memory SIMMs

Compatible Systems
- DEC Alpha
- Hewlett-Packard® HP®-700 Series
- 386/486/586/Pentium PC
- Silicon Graphics Indigo2™

Ordering Information

DESCRIPTION	MEMORY SIZE	ORDER NUMBER
EISA interface board with no media card	4 KB	H-AS-DEISA04K-00
	128 KB	H-AS-DEISA128-00
	512 KB	H-AS-DEISA512-00
	1 MB	H-AS-DEISA01M-00
	2 MB (4 LD SIMM)	H-AS-DEISAL2M-00
	2 MB (1 HD SIMM)	H-AS-DEISAH2M-00
	4 MB	H-AS-DEISA04M-00
	8 MB	H-AS-DEISA08M-00
EISA interface board with a coax media card	4 KB	H-AS-DEISA04K-10
	128 KB	H-AS-DEISA128-10
	512 KB	H-AS-DEISA512-10
	1 MB	H-AS-DEISA01M-10
	2 MB (4 LD SIMM)	H-AS-DEISAL2M-10
	2 MB (1 HD SIMM)	H-AS-DEISAH2M-10
	4 MB	H-AS-DEISA04M-10
	8 MB	H-AS-DEISA08M-10
EISA interface board with a standard fiber optic media card	4 KB	H-AS-DEISA04K-20
	128 KB	H-AS-DEISA128-20
	512 KB	H-AS-DEISA512-20
	1 MB	H-AS-DEISA01M-20
	2 MB (4 LD SIMM)	H-AS-DEISAL2M-20
	2 MB (1 HD SIMM)	H-AS-DEISAH2M-20
	4 MB	H-AS-DEISA04M-20
	8 MB	H-AS-DEISA08M-20
EISA interface board with a long-link fiber optic media card	4 KB	H-AS-DEISA04K-30
	128 KB	H-AS-DEISA128-30
	512 KB	H-AS-DEISA512-30
	1 MB	H-AS-DEISA01M-30
	2 MB (4 LD SIMM)	H-AS-DEISAL2M-30
	2 MB (1 HD SIMM)	H-AS-DEISAH2M-30
	4 MB	H-AS-DEISA04M-30
	8 MB	H-AS-DEISA08M-30